ECE/CS 552 Fall 2010:

Guideline for stage 2 project report

TA: Guangyu Shi

The general guideline for project report can be found on stage 2 project description – Section 4. This section is copy and pasted below:

Second Stage Project Report

The project should be done in a group of three. The second stage project report should emphasize the new elements that added to your design since the first stage of the project. The second stage project report should include the following parts:

1) A brief description of or an introduction to your project. Include a top-level schematic (if you write Verilog at top-level, you may draw a block diagram of you top-level design. Hand writing is okay.) Report its special features, any particular effort you have made to optimize the design, and any major problems you encountered in implementing the design.

2) A statement indicating whether or not your design meets all the requirements specified in this document.

3) Include schematic printouts or Verilog listings of major blocks that are not included in first stage project report.

4) The simulation results for test programs (will be provided later) in "list" form. Be sure to include the following signals:

   a. Instructions fetched from I-cache/memory.

   b. ALU operand, ALU result and ALU control signal (opcode).

   c. Register file read and write address and data; register control signal RegWrite.

   d. Memory read and write address and data; Memory control signal MemWrite (or WE).

   e. Data being written back at WB stage.

   These signals may come from the pipeline registers. Highlight the above signals, and add more in your simulation result if necessary.

5) A detailed description of the methodology you used to test the correctness of your design. Include a well commented copy of the key programs you used to create test inputs and/or verify the outputs from the various blocks.

6) If your project implements extra features (forwarding, etc.) that are not included in first stage project report, provide a short paragraph highlighting the extra features. Also, provide an estimate of performance enhancement due to these extra features for the testing program. Bonus point will not be considered if the design is incorrect.

In addition to the above requirement, here are the additional guidelines to make your report more readable:

1. No matter if your design is in schematic, HDL or combined, you must provide a top level schematic diagram in your report. If your top-level is written in HDL, you can draw a schematic diagram of your design by hand or using computer software.

2. The function blocks that appears in the first stage project report: if you did not revise them, you do not have to include them in the second stage report again.

3. Use both program c and d as your testbenches. You can add more if you want.

4. Simulation waveform: list the following signal in the specified order as follows:
1) Clock signal.
2) PC value.
3) Instructions from IF/ID the register.
4) Register read data a and b from the ID/EX register.
5) ALU result from EX/MEM register.
6) Write Data for memory writes, from the EX/MEM register.
7) Memory Address from the EX/MEM register.
8) Writeback result from the MEM/WB register (after the multiplexor).
These are the first 8 signal that should appear on your waveform. You may add more, but do not change the order. The values in the waveform must be READABLE.

5. You do not have to print out the whole wave form. Show us the following fractions of the waveform.
1) Initialization phase: Instruction 0-7 in program c, and 0-16 in program d.
2) One loop of computation, including jumping to the subroutine and returning from it.
3) Final result in the finishing stage. Highlight the EXEC instruction, its following (LW/ADD) instruction and the result of this instruction (in program c, the writeback result should be 6 and in program d, the writeback result should be 0x90).
You do not have to include waveforms on which the whole pipeline is stalled most of the time for serving cache misses. We want to see waveforms with information.

6. If your design was not functioning correctly in the demo, clearly state what kind of problem in your design causes the failure in running program d. Also state whether you are able to fix the problem in the final report and include simulation waveform to prove that.